**Amendments to the Claims**

Please amend Claims 1, 7, 12 and 18. The Claim Listing below will replace all prior versions of the claims in the application:

**Claim Listing**

What is claimed is:

1. (Currently amended) A packet buffer random access memory (PBRAM) device, comprising:

(a) a memory array divided into a plurality of banks;

(b) a plurality of input ports to be coupled to a network controller device, the memory array for storing packet data received by the plurality of input ports being shared by the plurality of input ports; [[and]]

(c) a plurality of serial registers each associated with a different one of the plurality of input ports, each of the serial registers configured for receiving packet data from the associated input port at a segment of a serial register concurrent with writing other packet data to the memory array [[at]] from another segment of the serial register, each of the serial registers further being segmented into a plurality of segments, segments of respective serial registers being associated with corresponding portions of the memory array, segments of different serial registers simultaneously transferring packet data to different portions of the memory array;

(d) row and column circuitry at each of the plurality of banks, the row and column circuitry configured to enable said writing other packet data to a respective bank independent of operation at other banks; and

(e) a plurality of multiplexers each associated with a different one of the segments of the serial registers, each multiplexer enabling said writing other packet data to the memory array from a respective segment of the serial register.

2. (Original) The PBRAM device of claim 1 wherein packet data is transferred into one segment of a serial register as data is simultaneously transferred out of another segment of the serial register.

3. (Original) The PBRAM device of claim 1 wherein a portion of the memory array is a queue.

4. (Original) The PRAM device of claim 3 wherein the queue includes a plurality of sub-queues, each sub-queue assigned a priority level.

5. (Original) The PBRAM device of claim 4 wherein packet data is read from the sub-queue with the highest priority level that stores data.

6. (Original) The PBRAM device of claim 1 wherein the memory array is a single global memory.

7. (Currently amended) A method for storing data packets transferred across a computer network in a packet buffer random access memory (PBRAM) device, the method comprising:

receiving a plurality of data packets from controllers coupled to said computer network at a plurality of input ports of the PBRAM device;

serially transferring portions of the data packets to different segments of serial registers that are connected between the input ports and a memory array divided into a plurality of banks, each of the serial registers being associated with a different one of the input ports, the memory array for storing packet data received by the input ports being shared by the plurality of input ports; [[and]]

selecting at least one of the plurality of banks to receive the portions of the data packets independent of other banks of the plurality of banks; and

conveying the portions of the data packets from one of the serial registers to different portions of the memory array in parallel, while concurrently transferring other portions of the packets to other segments of the one of the serial registers, said conveying

including multiplexing the portions of the data packets from respective segments of the serial registers onto a data bus.

8. (Original) The method of claim 7 wherein a portion of the memory array is a queue.

9. (Original) The method of claim 8 wherein the queue includes a plurality of sub-queues, each sub-queue assigned a priority level.

10. (Original) The method of claim 9 wherein packet data is read from the sub-queue with the highest priority level that stores data.

11. (Original) The PBRAM device of claim 7 wherein the memory array is a single global memory.

12. (Currently amended) A packet buffer random access memory (PBRAM) device comprising:

a memory array divided into a plurality of banks;

a plurality of input ports coupled to the memory array by serial registers for conveying data to the memory array, each of the serial registers being associated with a different one of the input ports and configured for receiving packet data from the associated input port to a segment of a serial register concurrent with writing other packet data to the memory array from another segment of the serial register, the memory array for storing packet data received by the plurality of ports being shared by the plurality of input ports;

row and column circuitry at each of the plurality of banks, the row and column circuitry configured to enable said writing other packet data to a respective bank independent of operation at other banks;

a plurality of multiplexers each associated with a different one of the segments of the serial registers, each multiplexer enabling said writing other packet data to the memory array from a respective segment of the serial register;

a plurality of command ports for receiving commands that indicate desired operations to be performed in relation to the data conveyed on the input ports; and

a memory management unit coupled between the command ports and the memory array, said memory management unit establishing input queue structures within the memory array responsive to write commands issued on the command ports, the input queue structures for receiving pointers to locations in a packet table that point to the data that is conveyed from the input ports.

13. (Original) The PBRAM device of claim 12 wherein the memory array is a single global memory.

14-17. (Cancelled)

18. (Currently amended) An apparatus for storing packets transferred across a computer network in a packet buffer random access memory (PBRAM) device, comprising:

means for receiving a plurality of packets from controllers coupled to said computer network by a plurality of input ports of the PBRAM device;

means for assigning input queue structures, contained in a memory array portion of the PBRAM device divided into a plurality of banks, to store packets, the memory array being shared by the plurality of input ports;

means for serially transferring portions of the packets to different segments of serial registers that are connected to the input ports and to the memory array, each of the serial registers associated with a different one of the input ports;

means for selecting at least one of the plurality of banks to receive the portions of the packets independent of other banks of the plurality of banks;

means for conveying the portions of the packets from a segment of a serial register to the memory array portion in parallel, concurrent with receiving other packet data to another segment of the serial register, said means for conveying including means for multiplexing the portions of the packets from respective segments of the serial registers onto a data bus; and

means for storing said packets in said queue structures, said queue structures being further accessible by a plurality of output ports of said PBRAM device such that said input queue structures become output queue structures that deliver the packets to associated output ports.

19. (Original) The apparatus of claim 18 wherein an output queue structure includes a plurality of sub-queues, each sub-queue assigned a priority level.

20. (Original) The apparatus of claim 19 wherein packet data is read from the sub-queue with the highest priority level that stores data.

21. (Original) The PBRAM device of claim 18 wherein the means for storing is a single global memory.

22-25. (Cancelled)